REMARKS

I. Formalities

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119 and for confirming receipt of the certified copy of the priority document.

Applicant thanks the Examiner for considering the references cited with the form PTO-1449 submitted with the Information Disclosure Statement filed on February 9, 2004.

Applicant thanks the Examiner for acknowledging the election without traverse of claims 12-15 in the Response to Restriction Requirement filed June 2, 2004.

Applicant thanks the Examiner for indicating that the Formal Drawings filed on February 9, 2004 are accepted.

II. Status of the Application

As an initial matter, Applicant notes that the Examiner has suggested that Applicant cancel claims 1-11 to avoid a double patenting situation if these claims remain pending for the current prosecution. However, Applicant has already canceled claims 1-11 with the Preliminary Amendment filed on February 9, 2004. Indeed, in the Office Action dated May 27, 2004, the Examiner acknowledged that claims 1-11 have been canceled. Accordingly, correction of this error is respectfully requested.

Claims 12-36 are all the claims pending in the Application. Claims 1-11 have been canceled and claims 16-36 have been withdrawn from further consideration. Claims 12-15 have been rejected.

The present amendment addresses each point of objection and rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

III. Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 12-15 under 35 U.S.C. § 103 as being unpatenable over U.S. Patent Publication No. 2004/0022249 A1 to Katayama et al. (hereinafter "Katayama"), in view of Applicant's admitted prior art. Applicant respectfully traverses this rejection for *at least* the reasons stated below.

Independent claim 12 requires (among other things):

> ...the substitution information for said first memory cell array being stored in said substitution information storing memory cells in said second memory cell array, the substitution information for said second memory cell array being stored in said substitution information storing memory cells in said first memory cell array...

The grounds of rejection allege that Applicant's admitted prior art teaches many of the features recited in claim 12, but fails to teach or suggest that the semiconductor memory includes first and second memory cell arrays, wherein substitution information for said first memory cell array is stored in said substitution information storing memory cells in said second memory cell array, and substitution information for said second memory cell array is stored in said substitution information storing memory cells in said first memory cell array, as required by claim 12.

Nevertheless, the grounds of rejection apply Katayama, taking the position that Katayama teaches or suggests this feature. Additionally, the grounds of rejection allege that one of skill

would have been motivated to combine Applicant's admitted prior art with Katayama so that faulty memory is prevented from being used.

Applicant respectfully disagrees with the Examiner. In order to establish a *prima facie* case of obviousness under 35 U.S.C.§ 103(a), the Examiner must show that the prior art references, when combined, teach or suggest all of the limitations of the rejected claim. *See* MPEP § 2143. However, the grounds of rejection do not show that Applicant's admitted prior art, Katayama, or any combination thereof, teaches or suggests all of the limitations of claims 12. Specifically, the grounds of rejection do not point to any portion of Applicant's admitted prior art or Katayama that provides any teaching or suggestion whatsoever that substitution information for a first memory cell array is stored in substitution information storing memory cells in a second memory cell array, and that substitution information for said second memory cell array is stored in substitution information storing memory cells in said first memory cell array, as required by claim 12.

Indeed, not only does claim 12 require the feature of substitution information for a first memory cell array being stored in a second memory cell array, claim 12 further requires that substitution information for said second memory cell array is stored in said first memory cell array. Neither Applicant's admitted prior art, Katayama, nor any combination thereof, teaches or suggests this feature.

In contrast to the requirements of claim 12, Katayama teaches that the inside of electrically reloadable nonvolatile memory 52 is divided into regions having a predetermined size. *See* paragraph 0079. Further, Katayama refers to each of such regions as "a block." *See*

paragraph 0079. In addition, Katayama teaches that a memory system may be organized into a first group of blocks, and a second group of blocks, wherein the second group of blocks is for storing information of the characteristics of said first group of blocks. *See e.g.*, claim 1. More particularly, Katayama teaches that the second group of blocks may store an indication of whether a corresponding block within said first group is defective or not, and that the second group of blocks may also store an address of a substitute block. *See e.g.*, claim 8.

However, Katayama provides no teaching or suggestion whatsoever that, in addition, substitution information for said second block, is stored in substitution information storing memory cells in said first block. In fact, Katayama teaches quite the opposite—that the first group of blocks is designated for storing user data and characteristics of the user data being written in said first block. *See* claim 1.

Further, the grounds of rejection do not provide any evidentiary support whatsoever as to any specific aspect of Applicant's admitted prior art or Katayama that teaches or suggests the feature of substitution information for a first memory cell array being stored in a second memory cell array, and substitution information for said second memory cell array being stored in said first memory cell array, as required by claim 12. Moreover, it would not have been obvious to one of ordinary skill to modify the teachings of Applicant's admitted prior art and Katayama to include such a feature. To the contrary, Katayama teaches away from such a modification, in that, Katayama teaches that the first group of blocks is designated for storing user data and characteristics of the user data being written in said first block. *See* claim 1. Absent a showing

that the prior art references, when combined, teach or suggest all of the limitations of claim 12, the Examiner has failed to establish a *prima facie* case of obviousness.

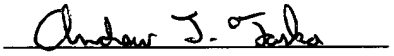
Accordingly, Applicant respectfully submits that independent claim 12 is patentable over Applicant's admitted prior art, Katayama, and any combination thereof, for *at least* these reasons. Further, Applicant respectfully submits that the dependent claims 13-15 are allowable, *at least* by virtue of their dependency on independent claim 12. Thus, Applicant respectfully requests that the Examiner withdraw this rejection.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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